tor the gate resonant circuit is a lumped element series resonant arrangement consisting of chip varactor, series wirebond, and the gate input impedance. The output drain circuit is a single section impedance transformer. Fig. 5 shows the tuning characteristic of this oscillator. The minimum output power and efficiency are 25 mW and 1.6 percent, respectively. Over most of the tuning range, the output power is in excess of 40 mW and the efficiency is greater than 3 percent.

V. Conclusions

It has been shown that, in a symmetrical FET structure, the roles of the source and drain ohmic contacts may be interchanged by reversing the source–drain bias polarity. In power oscillator applications, this allows the realization of an optimally heat-sunk flip-chip common-drain circuit. Using this technique, both single-frequency and varactor-tuned high-frequency oscillators have been realized. It is felt that this technique will find wide usage in microwave oscillators because of the simplicity of the approach and the high performance possible.

Acknowledgment

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11-GHz GaAs Power MESFET Load-Pull Measurements Utilizing a New Method of Determining Tuner *Y* Parameters

HIROYUKI ABE AND YOICHI AONO

***Abstract*—A load-pull technique utilizing a new method of determining tuner *Y* parameters is proposed for large-signal characterization of microwave power transistors. Large-signal input–output transfer characteristics of an active circuit containing a GaAs FET and an input matching circuit are measured by inserting a microstrip tuner between the active circuit output drain terminal and the 50-Ω load. The microstrip-tuner *Y* parameters are determined by comparing the dc bias-dependent small-signal *S* parameter S_{22} of the active circuit and that of the circuit which contains the active circuit and microstrip tuner. The reflection coefficient presented to the active circuit output drain terminal is derived from tuner *Y* parameters.**

Optimal load impedances for output power, obtained with this new load-pull technique, are used to design *X*-band GaAs FET power amplifiers. An 11-GHz power amplifier with a 3000-μm gate-width FET chip delivers 1-W microwave power output with 4-dB gain in the 500-MHz band.

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I. Introduction

IN DESIGNING power amplifiers, it is important to know the transistor load characteristics at a high input driving-power level and to optimize the output matching

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circuit on the basis of these large-signal characteristics. The load-pull technique is essential for this purpose. With the conventional technique, external tuners are adjusted, demounted, and measured. To avoid the unknown degree of error inherent in the conventional load-pull technique, the automatic load contour mapping technique [1], equivalent load-pull technique [2], and large-signal S-parameter characterization [3] have been proposed. However, these techniques require a complicated test fixture or repeated measurements of small-signal S parameters S_{11}, S_{12}, S_{21}, and S_{22} of a two-port circuit containing a transistor and tuners.

This paper describes a load-pull measurement technique utilizing a new method of determining the tuner Y parameters. Large-signal input–output characteristics of an active circuit containing a GaAs FET and an input matching circuit are measured by inserting a microstrip tuner between the active circuit output drain terminal and 50-Ω load. The microstrip tuner Y parameters are determined by comparing the dc bias-dependent small-signal S parameter S_{22} of the active circuit and that of the circuit containing the active circuit and microstrip tuner. The tuner Y parameters are determined by best fitting these two sets of S parameter S_{22}. The reflection coefficient Γ_x, presented to the active circuit by the microstrip tuner terminated with a 50-Ω load, is derived from the tuner Y parameters.

A simple computer program has been developed. Once the dc bias-dependent small-signal S parameter S_{22} of the active circuit is measured and stored in the memory, Γ_x is calculated by feeding into the program the measured small-signal S parameter S_{22} of the circuit containing the active circuit and microstrip tuner.

Using this new method of determining tuner Y parameters, the load reflection coefficient Γ_x can be measured without disconnecting the microstrip tuner from the active circuit. Furthermore, the measuring procedure is simpler than the large-signal S-parameter characterization cited above, because Γ_x is obtained only measuring dc bias-dependent small-signal S parameter S_{22}.

The new load-pull technique is applied to 11-GHz GaAs MESFET large-signal characterization and the relationship between the load reflection coefficient Γ_x and input–output transfer characteristics are obtained. Constant-power contours at 11.2 GHz and the frequency dependence of the optimal load impedance between 10.7 and 11.7 GHz are presented.

X-band GaAs power amplifiers are designed and fabricated on the basis of the transistor load characteristics obtained by the new load-pull technique. The microwave performance of the 11-GHz GaAs FET power amplifier with 1-W output are described.

II. Principle of Measurement

For load-pull measurement, an impedance tuner is inserted between the transistor output terminal and 50-Ω load, which represents the power measuring circuit. Microwave power is fed to the transistor input terminal through the input matching circuit, and power delivered to the load is measured. When reflection coefficient Γ_x, seen from the transistor output terminal (A-A') toward the load, is measured, a load-power characteristic is obtained. The new technique proposed here is concerned with the reflection coefficient Γ_x measurement. The principles of the new technique are schematically shown in Fig. 1.

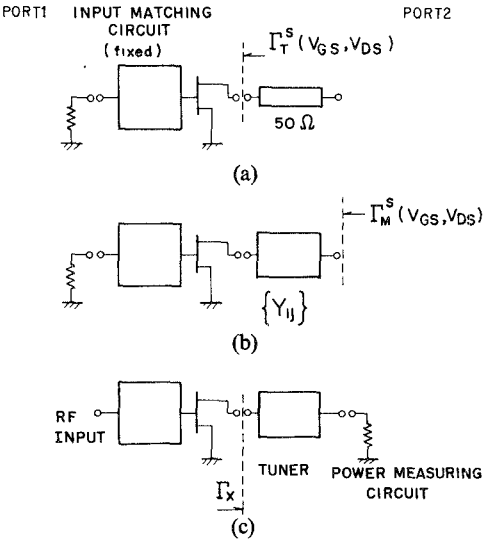


Fig. 1. New load-pull technique principle.

This new technique is developed from the simple concept that the dc bias-dependent small-signal S parameter $S_{22}^s=\Gamma_T^s$ of an active circuit, with a transistor and an input matching circuit, remains unchanged after the active circuit is connected to one of the ports of microstrip tuner. The small-signal reflection coefficient Γ_M^s seen at the other port of tuner, toward the transistor, is also dc bias-dependent. Γ_M^s and Γ_T^s for various drain–source bias voltages V_{DS} are shown in Fig. 2. If the matching tuner is represented by unknown two-port Y parameters $\{Y_{ij}\}$, admittances $Y_T^s(V_{GS},V_{DS})$ and $Y_M^s(V_{GS},V_{DS})$ obey the following equations:

$$Y_M^s(V_{GS},V_{DS})=Y_{22}-\frac{(Y_{12})^2}{Y_{11}+Y_T^s(V_{GS},V_{DS})} \tag{1a}$$

$$Y_T^s(V_{GS},V_{DS})=Y_0\frac{1-\Gamma_T^s}{1+\Gamma_T^s} \tag{1b}$$

$$Y_M^s(V_{GS},V_{DS})=Y_0\frac{1-\Gamma_M^s}{1+\Gamma_M^s}, \qquad Y_0=20\ \text{m℧}. \tag{1c}$$

Equation (1a) can be transformed into the following equation:

$$(Y_T^s(V_{GS},V_{DS})+Y_{11})(Y_M^s(V_{GS},V_{DS})-Y_{22})+(Y_{12})^2=0. \tag{1a'}$$

When the sets of Y_T^s and Y_M^s are measured at N bias points, tuner two-port parameters $\{Y_{ij}\}$ are determined so as to minimize the following error function F:

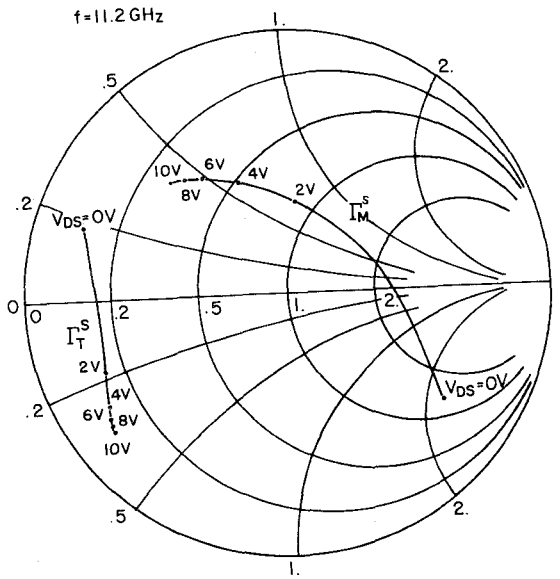


Fig. 2. Reflection coefficients at 11.2 GHz, dependent on the drain–source bias voltage V_{DS}. Γ_T^s: small-signal reflection coefficient seen at the transistor drain terminal. Γ_M^s: small-signal reflection coefficient seen from outside the microstrip tuner. The gate–source bias voltage is fixed at $V_{GS}=3$ V. $Z_0=50\ \Omega$.

$$F=\sum_{n=1}^{N}\left|\{Y_T^s(V_{GS}^{(n)},V_{DS}^{(n)})+Y_{11}\}\cdot\{Y_M^s(V_{GS}^{(n)},V_{DS}^{(n)})-Y_{22}\}+(Y_{12})^2\right|^2 \quad (2)$$

where $V_{DS}^{(n)}$ and $V_{GS}^{(n)}$ are the drain–source bias voltage and the gate–source bias voltage at the nth bias point. Once Y parameters $\{Y_{ij}\}$ are known, the reflection coefficient Γ_x is derived by the following equation:

$$\Gamma_x=\frac{Y_0-Y_L}{Y_0+Y_L}$$

$$Y_L=Y_{11}-\frac{(Y_{12})^2}{Y_0+Y_{22}}. \quad (3)$$

When the matching tuner can be assumed to be reactive, Y parameters are expressed by only three real parameters A, B, and C:

$$\{Y_{ij}\}=\begin{pmatrix} jA & jB \\ jB & jC \end{pmatrix}. \quad (4)$$

In this case, $N=2$ is sufficient to determine the three parameters.

The algorithm for calculating Γ_x from measured Γ_M^s and Γ_T^s is described in the Appendix.

III. Measurement Procedure

A microstrip tuner, as shown in Fig. 3, has been developed for this load-pull technique. It contains a 50-Ω microstrip line and bonding pads of metal layer (shaded parts). This microstrip tuner is inserted between the source-grounded FET drain terminal and output connector. By bonding gold tapes between the pads and the 50-Ω line, output tuning can be realized. A two-step matching circuit is attached at the FET gate terminal. This matching circuit contains ceramic capacitors [4] and microstrip stubs. Numerical values for input matching circuit elements are determined with computer aids by using the small-signal transistor S parameter S_{11} so as to minimize input VSWR's within the operating bandwidth. There are three steps for measurement.

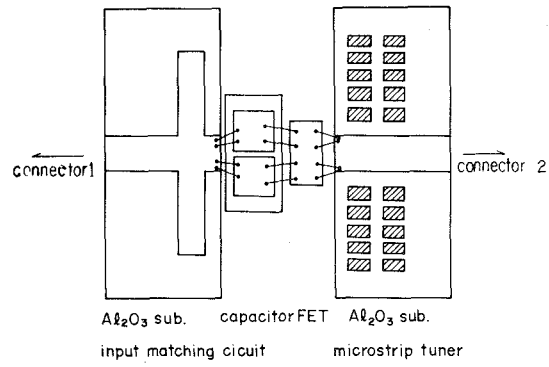


Fig. 3. Microstrip tuner and input matching circuit.

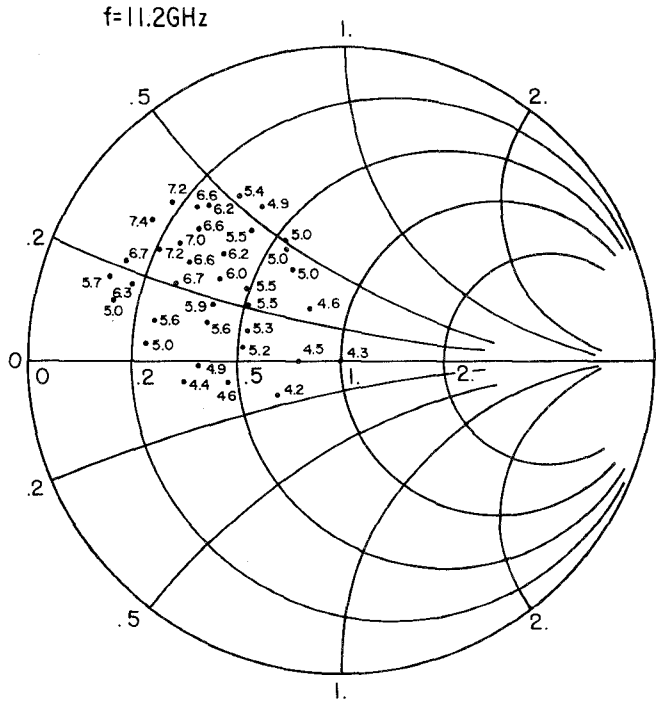
1) Connector 1 is connected to the external bias network terminated with a 50-Ω load. Without any tuning at the output port, transistor small-signal reflection coefficients Γ_T^s are measured on a network analyzer at $(V_{GS},V_{DS})=(3\text{ V},10\text{ V})$ and $(V_{GS},V_{DS})=(3\text{ V},0\text{ V})$ (Fig. 1(a)).

2) Gold tapes are bonded so as to realize a nonzero reflection coefficient to the transistor drain terminal. Next, reflection coefficient Γ_M^s is measured at the same bias points as in the first step. Then Γ_T^s and Γ_M^s are put into the computer program, and microstrip tuner Y parameters $\{Y_{ij}\}$ and Γ_x are calculated by the principle described in the second section (Fig. 1(b)).

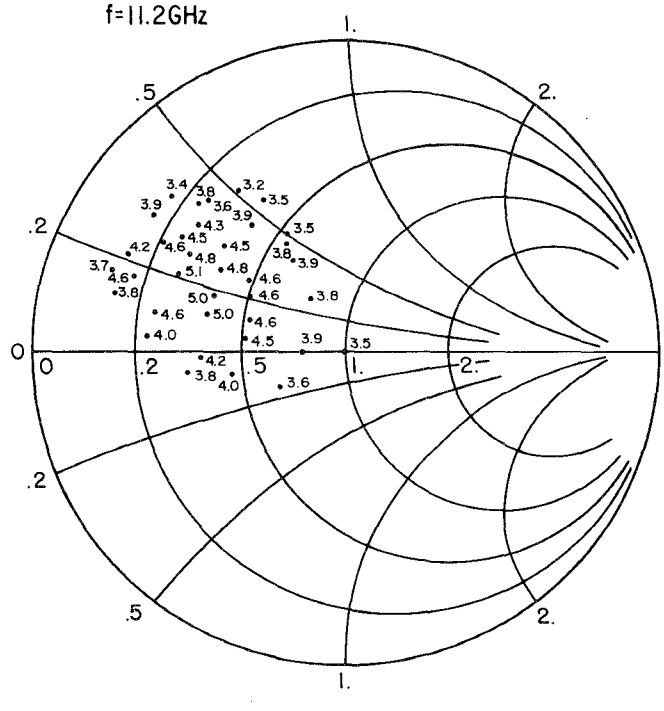
3) Connector 1 is connected to a signal generator through a bias network, and connector 2 is connected to a power meter through another bias network. DC bias is provided through bias networks, and large-signal input–output transfer characteristics are measured (Fig. 1(c)).

The gold tape positioning determines various reflection coefficients Γ_x given to the transistor drain terminal. The relationships between Γ_x and gain of an amplifier with 1500-μm gate-width GaAs FET are shown in Fig. 4(a) and (b). The location of the points shows the Γ_x, and the number beside the points shows the gain. The input driving power levels are 15 dBm (Fig. 4(a) and 23 dBm (Fig. 4(b)). From gain-Γ_x plotting, constant-gain contours are derived.

Constant-gain contours of an amplifier with 1500-μm gate-width GaAs FET at $(V_{GS},V_{DS})=(3\text{ V},10\text{ V})$ are shown in Fig. 5. Input driving levels are 15 and 23 dBm. It is clearly shown that the optimal load impedance deviates from the complex conjugate of S_{22}^s as the input driving level increases. To design wide-band amplifiers, large-signal load characteristics are obtained at several



(a)



(b)

Fig. 4. Gain-Γ_x characteristics of an amplifier with a 1500-μm gate-width GaAs FET: $(V_{GS}, V_{DS})=(3\text{ V}, 10\text{ V})$, $Z_0=50\ \Omega$.

frequencies within the operating bandwidth. Optimal load impedances at 10.7, 11.2, and 11.7 GHz are shown in Fig. 6. Input driving levels are 23 dBm for an amplifier with a

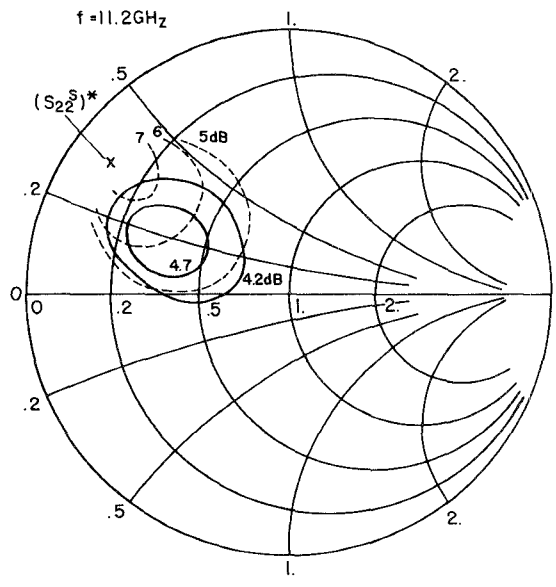


Fig. 5. Constant gain contour at 11.2 GHz. Input driving levels are 15 and 23 dBm. The GaAs FET gate width is 1500 μm. $(V_{GS}, V_{DS})=(3\text{ V}, 10\text{ V})$, $Z_0=50\ \Omega$.

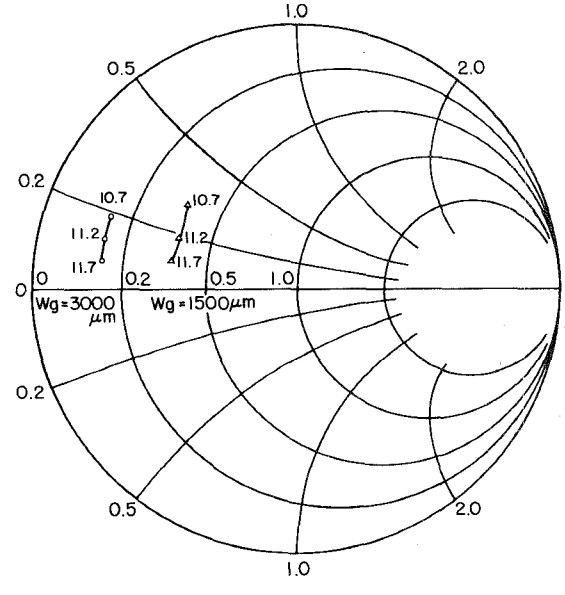


Fig. 6. Optimal load impedances at 10.7, 11.2, and 11.7 GHz. The GaAs FET gate widths are 1500 and 3000 μm. $(V_{GS}, V_{DS})=(3\text{ V}, 10\text{ V})$, $Z_0=50\ \Omega$.

1500-μm gate-width FET and 26 dBm for an amplifier with a 3000-μm gate-width FET.

IV. 11-GHz GaAs FET Amplifier

GaAs FET power amplifiers in the 11-GHz band were designed based on the large-signal load characteristics [5] and fabricated. The output matching circuits are designed with computer aid on the basis of frequency-dependent optimum load impedance $Y_{oL}(f_l)$ $(l=1,2,\cdots,L)$, where f_l's are frequencies within a specified frequency band. In the output matching circuit CAD, parameters $\{x_1, x_2, \cdots,$

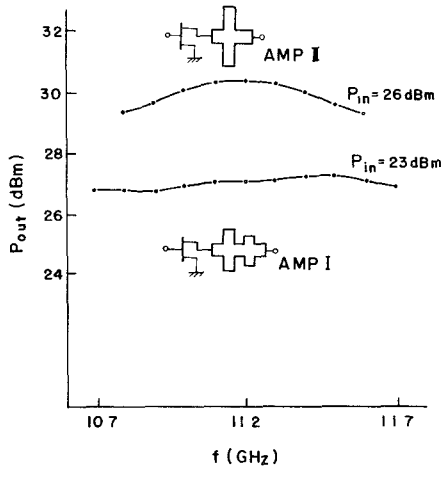


Fig. 7. Output power response versus frequency of amplifiers I and II. Amplifier I (with 1500-μm FET): (V_{GS}, V_{DS})=(3 V, 10 V), $I_{DS}\simeq$170 mA. Amplifier II (with 3000-μm FET): (V_{GS}, V_{DS})=(3 V, 12 V), $I_{DS}\simeq$420 mA.

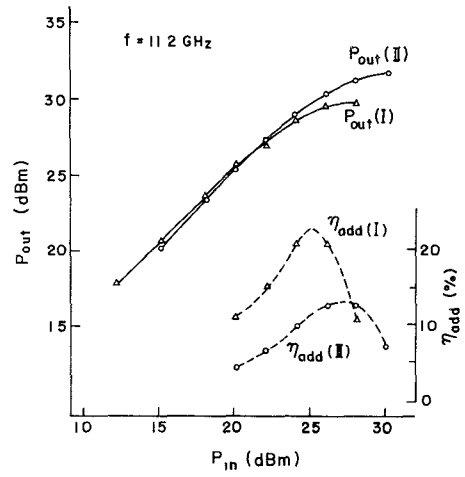


Fig. 8. Input and output transfer characteristics of amplifiers I and II dc biases are the same as in Fig. 7.

$x_k\}$, representing the position, characteristic impedance, and length of microstrip stubs, are determined so as to minimize the following trial function:

$$F_T = \sum_{l=1}^{L} |Y_{ms}(f_l) - Y_{oL}(f_l)|^2 \tag{5a}$$

$$Y_{ms}(f_l) = Y_{11}(f_l, \{x_k\}) - \frac{(Y_{12}(f_l, \{x_k\}))^2}{Y_0 + Y_{22}(f_l, \{x_k\})} \tag{5b}$$

where Y_{11}, Y_{12} $(= Y_{21})$, and Y_{22} are matching circuit Y parameters expressed as functions of parameters $\{x_k\}$.

A 1500-μm gate-width FET chip used in amplifier I and a 3000-μm gate-width FET chip used in amplifier II were obtained from the same wafer as FET chips used in the large-signal characterization. The GaAs FET has a submicrometer gate. The detailed structure is described elsewhere [6]. Amplifier I has a two-step matching element, and amplifier II has a one-step matching element as shown schematically in Fig. 7. The length and position of microstrip stubs were determined to make the output power level ripple as small as possible within the operating bandwidth. Output power responses versus frequency of amplifiers I and II are shown in Fig. 7. The FET gate–source bias voltages are 3 V, which is nearly equal to half-pinch-off voltage. The drain–source bias voltages are 10 and 12 V, which are less than half the drain–source breakdown voltage. At 23-dBm input driving level, amplifier I output power level is 27 ± 0.3 dBm within the 1-GHz band (10.7–11.7 GHz). Amplifier II delivers 30 ± 0.5 dBm within an 800-MHz band (10.8–11.6 GHz) when driven at a 26-dBm input level. Input–output transfer characteristics are shown in Fig. 8. Small-signal gains are 5.3 dB (amplifier I) and 4.8 dB (amplifier II). Saturated power levels are 0.92 W (29.6 dBm) and 1.5 W (31.6 dBm).

V. Conclusion

The new load-pull technique, in which dc bias-dependent transistor small-signal impedances are used as references, is shown to provide a precise and convenient procedure for transistor large-signal characterization. By using the technique, constant power contours are drawn on a Smith chart for various driving levels. The optimal load impedances measured by this technique are used for power amplifier design.

An 11-GHz power amplifier using a GaAs FET chip with a simplified recess structure delivers 1-W output power. The amplifiers have sufficient microwave performances for communication and broadcasting systems at frequencies higher than 10 GHz.

Appendix

Algorithm for Calculating Γ_x

The small-signal admittances Y_T^s and Y_M^s are calculated from measured Γ_T^s and Γ_M^s by (1b) and (1c). Y_T^s and Y_M^s are expressed as complex numbers:

$$Y_T^s(V_{GS}^{(n)}, V_{DS}^{(n)}) = p_n + jq_n \tag{A1}$$

$$Y_M^s(V_{GS}^{(n)}, V_{DS}^{(n)}) = u_n + jv_n \qquad (n=1,\cdots,N). \tag{A2}$$

By putting $D = AC - B^2$, F is expressed as a function of A, C, and D:

$$F = \sum_{n=1}^{N} \left[(-Av_n + Cq_n + D + p_n u_n - q_n v_n)^2 + (Au_n - Cp_n + q_n u_n + p_n v_n)^2 \right]. \tag{A3}$$

The values of A, C, and D which minimize F can be obtained as a solution to the following simultaneous linear equations:

$$\frac{\partial F}{\partial A} = \sum_{n=1}^{N} \left[-2v_n(-Av_n + Cq_n + D + p_n u_n - q_n v_n) + 2u_n(Au_n - Cp_n + q_n u_n + p_n v_n) \right] = 0 \tag{A4}$$

$$\frac{\partial F}{\partial C} = \sum_{n=1}^{N} \left[2q_n(-Av_n + Cq_n + D + p_n u_n - q_n v_n) - 2p_n(Au_n - Cp_n + q_n u_n + p_n v_n) \right] = 0 \tag{A5}$$

$$\frac{\partial F}{\partial D} = \sum_{n=1}^{N} \left[2(-Av_n + Cq_n + D + p_n u_n - q_n v_n) \right] = 0. \tag{A6}$$

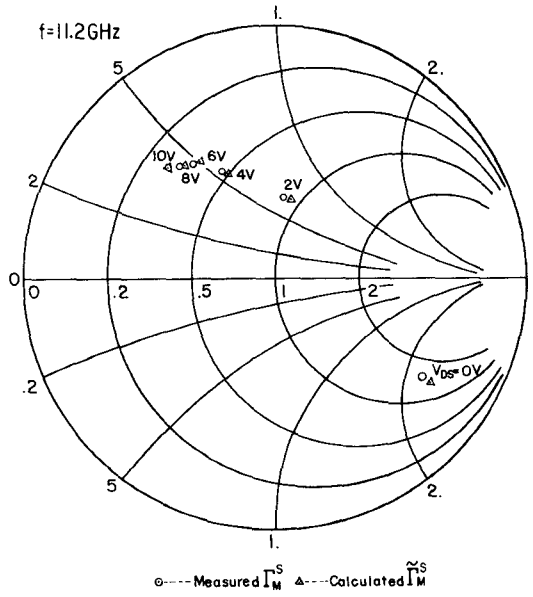


Fig. 9. Measured and calculated reflection coefficient Γ_M^s and Γ_M^s $V_{GS}=3$ V, $Z_0=50\ \Omega$.

In order for these simultaneous equations to have a nontrivial solution, N has to be larger than 2.

By solving these equations, parameters A, C, and B $(=\sqrt{AC-D})$ are obtained. The load reflection coefficient Γ_x is derived by the following equations:

$$Y_L = jA + \frac{B^2}{Y_0 + jC} \tag{A7}$$

$$\Gamma_x = \frac{Y_0 - Y_L}{Y_0 + Y_L}. \tag{A8}$$

As a numerical example, $\Gamma_T^s(V_{GS}=3\ \text{V}, V_{DS}=0\ \text{V})$, $\Gamma_T^s(V_{GS}=3\ \text{V}, V_{DS}=10\ \text{V})$ $\Gamma_M^s(V_{GS}=3\ \text{V}, V_{DS}=0\ \text{V})$ and $\Gamma_M^s(V_{GS}=3\ \text{V}, V_{DS}=10\ \text{V})$ that are shown in Fig. 1 are inputted to the program. This means that N equals 2. The following values are obtained for A, C, and B^2:

$$A=-1.84$$

$$C=-0.55$$

$$B^2=4.69 \qquad \text{(normalized by } Y_0=20\ \text{m℧)}.$$

To show how precisely these numerical values of A, C, and B represent the tuner characteristics, $\tilde{\Gamma}_M^s(V_{GS}, V_{DS})$ is calculated by the following equations:

$$\tilde{Y}_M^s(V_{GS}, V_{DS}) = jC + \frac{B^2}{Y_T^s(V_{GS}, V_{DS}) + jA}$$

$$\tilde{\Gamma}_M^s(V_{GS}, V_{DS}) = \frac{Y_0 - \tilde{Y}_M^s(V_{GS}, V_{DS})}{Y_0 + \tilde{Y}_M^s(V_{GS}, V_{DS})}$$

where $V_{GS}=3$ V and $V_{DS}=0$, 2, 4, 6, 8, and 10 V. The calculated $\tilde{\Gamma}_M^s$ is plotted in Fig. 9 along with the measured Γ_M^s.

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